WEB-6681 Series

VIA C3 Ezra/Eden

Embedded Board Computer

User's Manual

P/N: 205-00WEB66810, Version 1.0

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（**To Be Added**）

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How to Use This Manual

This manual is written for the system integrator, PC technician and knowledgeable PC end user. It describes how to configure your WEB-6681 Series to meet various operating requirements. The user's manual is divided into four chapters, with each chapter addressing a basic concept and operation of the server board.

Chapter 1: Introduction - presents what you have inside the box and gives you an overview of the product specifications and basic system architecture for the WEB-6681 Series server board.

Chapter 2: Hardware Configuration Setting - shows the definitions and locations of Jumpers and Connectors so that you can easily configure your system.

Chapter 3: System Installation - describes how to install this embedded computer board. It will also introduce and show you the driver installation procedure for the Graphics Controller and Ethernet Controller.

Chapter 4: BIOS Setup Information - specifies the meaning of each setup parameter, how to get advanced BIOS performance and update to a new BIOS. Additionally, the POST checkpoint list will give you a guide for troubleshooting.

The contents of this manual are subject to change without prior notice. These changes will be incorporated in new editions of this manual. We may make supplements or changes for the product described in this manual at any time.

Chapter 1 Introduction

WEB-6681 Series is a 5.25" embedded board computer with an on-board, embedded low power VIA C3 EZRA or EDEN-series processor. Other on-board features include chipsets built-in AGP 4x graphic core with CRT display, onboard 64MB system memory and a SO-DIMM socket for expansion and Triple 10/100 Mbps PCI Ethernet interfaces. A PC/104 expansion connector is provided, and SSD supports for one compact flash interface. Watchdog timer is from 1 second to 63 seconds and Hardware Monitoring is supported also.

EBC - VIA EDEN Platform

With this board, system engineers are able to develop the Web server system for some network appliances such as Fire-wall, VPN and Gateway. WEB-6681 Series, most scaleable x86 embedded platform, with low-power consumption highest performance is designed mainly for the rapidly emerging Connected Digital Information. VIA C3 EZRA or EDEN-series processors are specially designed to work well in environments with operating temperature up to 60℃ within this low power EBC significantly increases both MTBF and application possibilities.

1.1 Check List

The WEB-6681 Series package includes the following basic items accompany with this manual.

* One WEB-6681 Series embedded board computer
* One printer port cable kit
* One serial port cable
* Two IDE cables
* One 6-pin Keyboard and Mouse cable for min DIN

* One PS/2 Y-type cable
* One USB cable
* One CD-Title to support internal VGA display driver, IDE driver and Intel 82559 / Intel 82559ER / Realtek 8100B(L) network controller driver.

If any of these items is damaged or missed, please contact your vendor and save all packing materials for future replacement and maintenance.

1.2 Product Specification

Features

- 5.25" Embedded Board Computer
- Onboard VIA C3 EZRA 800AMHz or EDEN 400MHz
- Integrated AGP 4X 2D/3D Graphics core
- Support CRT and TFT panels
- Support Compact Flash Storage
- Support Triple 10/100Base-T fast Ethernets
- Support Ultra DMA 100/66/33 PCI-EIDE interface
- 1 COMs/1 Parallel/2 USBs

Specification

- **Chipset** : VIA VT8601A and VT82C686B
- **CPU**
  - Support VIA C3 EZRA <EBGA> and EDEN series processors
  - Onboard VIA C3 EZRA 800AMHz for Model: WEB-6681 Series ***X***-P800 series
  - Onboard VIA EDEN 400MHz for Model: WEB-6681 Series ***X***-P400 series
  - CPU bus clock : 66/100/133 MHz

- **L2 Cache Memory : CPU Integrated**
- **Main Memory**
  - Onboard 64MB SDRAM system memory, option for expansion to 128MB
  - One 144-pin SO-DIMM sockets
  - 32 MB to 512 MB
  - Supports up to double-sided or single-sided SO-DIMMs at 133/100 MHz system memory bus.
- **System BIOS**
  - AMI BIOS
  - 2MB Flash ROM for easy upgrades
  - Support ACPI, DMI, PnP, and Green function
- **IDE Interface**
  - Two enhanced IDE interface up to Four IDE devices with Ultra DMA 33/66/100
  - One IDE is 40-pin 2.54mm port; the other is 44-pin 2.00mm port, shared with the Compact Flash interface. Compact Flash interface is defined as master device; 44-pin IDE port is defined as slave device.
- **I/O Interface**
  - Parallel Port: Support one SPP, EPP/ECP bi-directional parallel port
  - Serial Ports: Support one RS232 port for COM1
- **Keyboard and PS/2 Mouse Interfaces**

  Support one connectors for Keyboard and Mouse
- **USB**

  Support 2 USB ports
- **Battery**

  Lithium battery
- **Real-Time Clock/Calendar (RTC)**

- Build-in VIA VT686B
- Y2K compliant

- **Watch-Dog Timer**

  From 1 to 63 seconds, software programmable

- **System Monitoring and Protection**
  - Monitoring system temperature, voltage, and cooling fan status
- **On-chip 3D AGP 4X VGA Display**
  - Integrated AGP 4X graphics core
  - Shared system memory up to 8MB Frame Buffer
  - One connector for CRT display interface
  - Support TTL LCD Panel
- **On-board Ethernet Function**
  - Triple Ethernet LAN controller
  - Realtek 8100B(L) for WEB-6681 SERIES SERIESR series and Intel 82559(ER) for WEB-6681 SERIES SERIESI series
  - Support Three 10/100BASE-T with RJ-45 connector
- **SSD Interface**
  - One socket supports Compact Flash Disk (type II)
  - Not support hot swap Mode
- **Expansion slot**
  - PC/104 ISA-bus connector for PC/104 module expansion
- **Mechanical and Environmental**
  - Outline Dimension (L X W): 203mm (8 inch) X 146m (5.75 inch)
  - PCB layout : 6-layer (Double-side components)
  - Power Requirements: ATX power
  - Operating Temperature : 0 ~ 60℃
  - Relative Humidity: 5% to 95%, non-condensing

1.3 System Architecture

The following illustration of block diagram will show you how WEB-6681 Series give you a highly integrated system solution. The most up-to-date system architecture of WEB-6681 Series include two main VLSI chips, VT8601A North Bridge and VT82C686B South Bridge, to support VIA EDEN/EZRA processor, SDRAM with non ECC, PCI bus interface, ACPI compliant power management, USB port, SMBus communication, and Ultra ATA/33/66/100 IDE Bus Master. The VT82C686B South Bridge will support PS/2 Keyboard/Mouse, one UARTs and Parallel. Besides, VGA is integrated in VT8601A North Bridge. Triple Ethernet devices will provide user more flexibility and reliability in a highly integrated application.

WEB-6681 Series are built-in VIA C3 EDEN or EZRA processors for high performance and cost-effective application. The North Bridge VT8601A provides a completely integrated solution for the system controller and data path components in a processor system. The South Bridge, VT82C686B, provides PCI-to-ISA bridge solution for the best industry application. It supports Ultra ATA 33/66/100 IDE master interface, full Plug-and-Play compatibility, and Advanced Programmable Interrupt Controller (APIC) interface on WEB-6681 Series`. It also supports 2-port Universal Serial Bus (USB), and internal Real-time Clock (RTC) to maintain date and time of a system.

The South Bridge VT82C686B, which integrates one high-speed serial ports, one parallel port, 8042 keyboard controller with PS/2 mouse ports. This parallel port supports one PC-compatible printer port (SPP), Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). Beside, it offer H/W monitor function.

VT82C686B standard 16-bit ISA bus slot is applied for all of slower I/O operations. In WEB-6681 Series, it contains Watch-dog Timer (WDT) Enabled by jumper setting and trigger by software. The on-board AGP device, graphics display port. The on-board PCI device, Triple Ethernet controllers, powered by Intel 82559

or Intel 82559(ER) or Realtek RTL8100BL supports 10/100 BASE-T data transfer.

All of details operating relations are shown in Figure 1-1 WEB-6681 Series System Block Diagram.

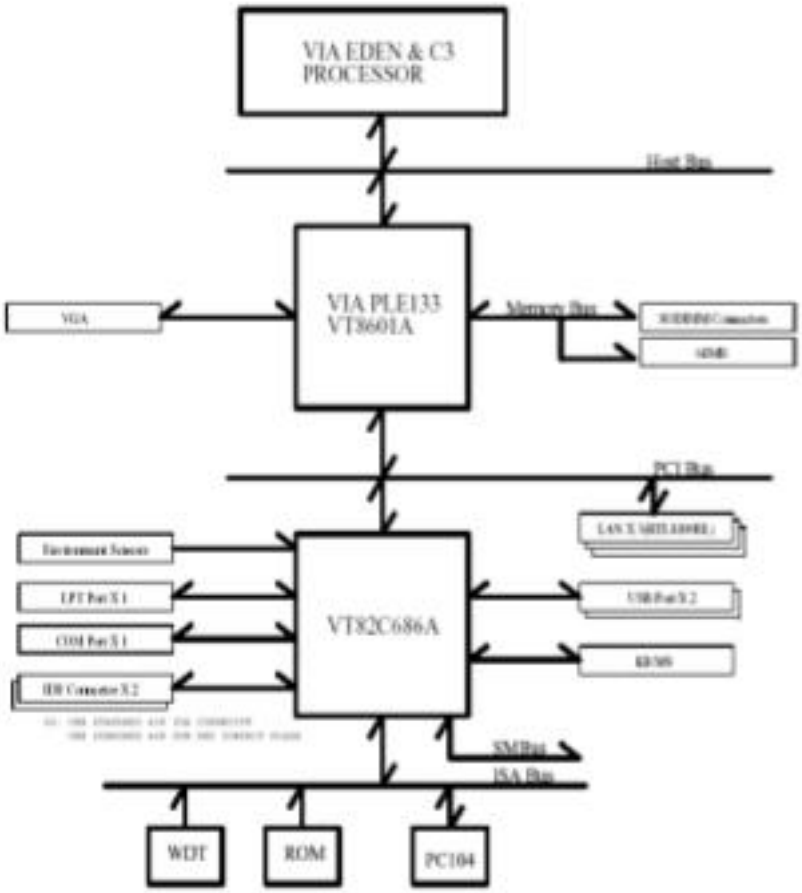


Figure 1-1 WEB-6681 Series System Block Diagram

Chapter 2 Hardware Configuration Setting

2.1 Jumper Notes

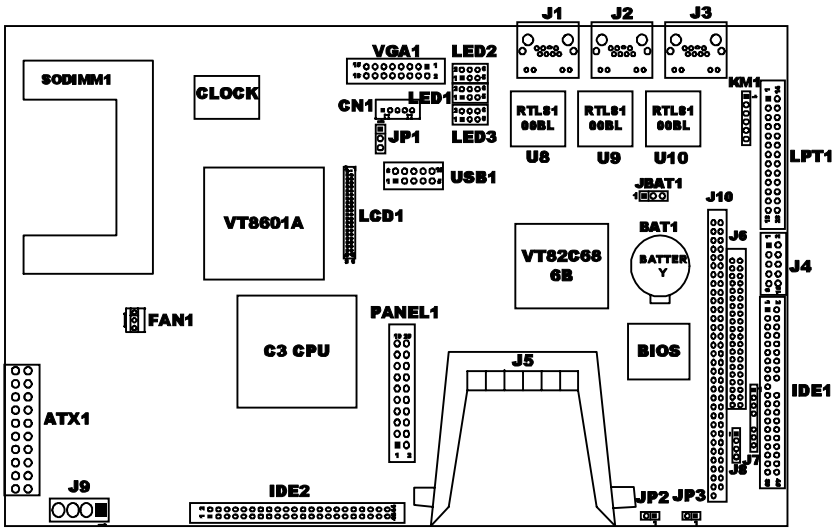
To close or Enabled a setting, put a jumper cap over the jumper pins. To open or disable a setting, make sure there is no jumper cap covering the jumper pins. See the table below for an illustration.

Notation	Description	Illustration
CLOSE	Pins 1 & 2 closed	
OPEN	Pins 1 & 2 open	
2-3	Pins 2 & 3 closed	

Table Jumper Setting Example

Note : In this chapter, settings which are marked with ♣ are default factory settings.

2.2 Jumper Locations



2.3 CMOS Content Trigger : JBAT1

The contents of the CMOS RAM can be cleared by shorting JBAT1 jumper for about 1 to 2 seconds. You should make sure that there is no power when clearing the CMOS RAM contents.

Description	JBAT1	Illustration
Normal operation ♣	1-2	
Clear CMOS content	2-3	

Table 1-1 Clearing CMOS Content (JBAT1)

2.4 Watching Dog Setting : JP2

Description	JP2	Illustration
WDT Enabled♣	CLOSE	
WDT Disable	OPEN	

Table 1-2 WDT Setting (JP2)

2.5 Watching Dog Address: JP3

Description	JP3	Illustration
PORT 443 ♣	CLOSE	
PORT 543	OPEN	

Table 1-3 WDT Adress(JP3)

2.6 LAN Status Indicators: LED1, LED2, LED3

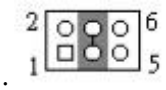
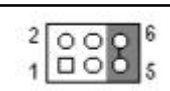
Description	LED1 LED2 LED3	Illustration
Active LED	1-2	
Link LED	3-4	
100/10 LED	5-6	

Table 1-4 Lan LED(Intel 82559 and RTL8100BL) Status(LED1,LED2,LED3)

2.7 Connectors

The connectors on the WEB-6681 Series are used to connect external devices such as hard disk drives, printers, keyboard, CRT, panel, serial ports, etc.

Specifically, WEB-6681 Series has the following connectors:

Connector	Description
J1,J2,J3	RJ45 Connector(Lan3,Lan1,Lan2)
ATX1	ATX Power Control
VGA1	VGA CRT Connector
J4	Serial Port Connectors
LPT1	Parallel Port Connector
KM1	PS/2 KB/MS Connector
J9	Power Connector
IDE1	IDE Connectors
SO-DIMM1	SO-DIMM Connector
USB1	USB Connectors
PANEL1	Front Bezel Connectors
J8	-5V ,–12V Power Connector
J5	Compact Flash Connector
IDE2	Disk On Module Connector
LCD1	TFT LCD Interface
CN1	TFT LCD Power Connector
J6,J10	PC104 Connector
BAT1	Battery socket

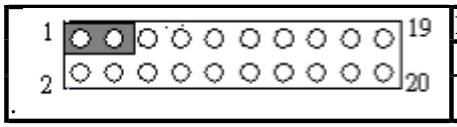
2-7-1 Front Bezel Connectors : PANEL1

The front bezel of the chassis has a control panel which provides light indication of the computer activities and switches to change the computer status. This is a 20-pin header that provides interfaces for the following

functions: Power LED, Hard Disk LED, Reset Switch and External Speaker.

(1) HDD LED : Pins 1 and 3

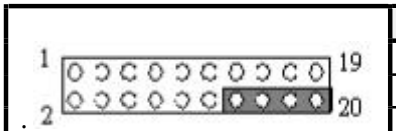
This connector connects to the Hard Drive activity LED on the control panel. This LED will flash when the HDD is being accessed.



Pin	Function
1	VCC
3	HDD-LED

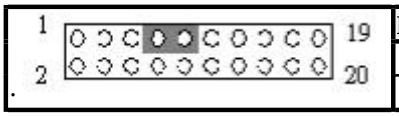
(2) External Speaker : Pins 14,16,18 and 20

This connector provides an interface to a speaker for audio tone generation. An 8-ohm speaker is recommended.



Pin	Function
14	VCC
16	GND
18	NC
20	SPEAK

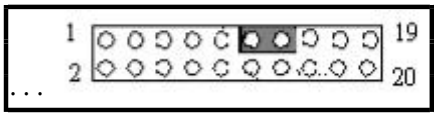
(3) Power Switch : Pins 7 and 9



Pin	Function
7	PW-BN
9	GND

(4) Power LED : Pins 11 and 13

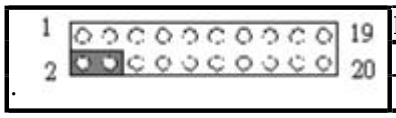
The power LED indicates the status of the main power.



Pin	Function
11	PW-LED
13	GND

(5) Reset Switch : Pins 2 and 4

The reset switch allows the user to reset the system without turning the main power switch off and then on.



Pin	Function
2	RSTSW
4	GND

2-7-2 PC104 BUS Connector : J6,J10

J6 and J10 are dual-in-line pin headers that support PC/104 modules. J10 consists of 64 pins (A12~A32, B1~B32). J6 has 40 pins (C1~C20, D1~D20). Their pin assignments are listed in the following tables.

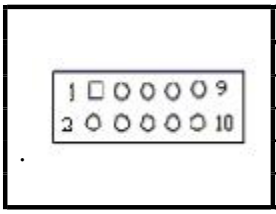
Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	IOCHK	A17	A14	B1	GND	B17	DACK1
A2	D7	A18	A13	B2	REST	B18	DRQ1
A3	D6	A19	A12	B3	VCC	B19	REFRESH
A4	D5	A20	A11	B4	IRQ9	B20	CLK
A5	D4	A21	A10	B5	-5V	B21	IRQ7
A6	D3	A22	A9	B6	DRQ2	B22	IRQ6
A7	D2	A23	A8	B7	-12V	B23	IRQ5
A8	D1	A24	A7	B8	OWS	B24	IRQ4
A9	D0	A25	A6	B9	+12V	B25	IRQ3
A10	IOCHRDY	A26	A5	B10	GND	B26	DACK2
A11	AEN	A27	A4	B11	SMEMW	B27	TC
A12	A19	A28	A3	B12	SMEMR	B28	BALE
A13	A18	A29	A2	B13	IOW	B29	VCC
A14	A17	A30	A1	B14	IOR	B30	OSC
A15	A16	A31	A0	B15	DACK3	B31	GND
A16	A15	A32	GND	B16	DRQ3	B32	GND

Pin	Function	Pin	Function	Pin	Function	Pin	Function
C1	GND	C11	MEMW	D1	GND	D11	DACK5
C2	SBHE	C12	D8	D2	MEMCS16	D12	DRQ5
C3	LA23	C13	D9	D3	IOCS16	D13	DACK6
C4	LA22	C14	D10	D4	IRQ10	D14	DRQ6
C5	LA21	C15	D11	D5	IRQ11	D15	DACK7

C6	LA20	C16	D12	D6	IRQ12	D16	DRQ7
C7	LA19	C17	D13	D7	IRQ15	D17	VCC
C8	LA18	C18	D14	D8	IRQ14	D18	MASTER
C9	LA17	C19	D15	D9	DACK0	D19	GND
C10	MEMR	C20	NC	D10	DRQ0	D20	GND

2-7-3 USB Connectors : USB1

This is a connector for Universal Serial Bus (USB1) ports. Pins 1-4 are used for the first port; pins 6-9 are used for the second port.



Pin	Function	Pin
1	Vcc	10
3	USB-	8
5	USB+	6
7	GND	4
9	Chassis GND	2

2-7-4 ATX Power Connector ATX1

Signals	ATX
+12V	10
+5V	4,6,19,20
-12V	12
-5V	18
5VSB	9
PS-ON	14
POWER-ON	8
Ground	3,5,7,13,15,16,17

2-7-5 KB/MS Connector : KM1

This is a 6-pin KB/MS Connector; it is also used as a 6-pin cable connector.

Pin	Function
1	KB_DATA
2	MS_DATA
3	GND
4	VCC
5	KB_CLK
6	MS_CLK

2-7-6 IDE Connectors : IDE1

IDE1 are EIDE connectors. IDE1 is for connecting primary IDE devices.

Pin	Function	Pin	Function
1	Reset IDE	21	DRQ0
2	Ground	22	Ground
3	Host data 7	23	Host IOW
4	Host data 8	24	Ground
5	Host data 6	25	Host IOR
6	Host data 9	26	Ground
7	Host data 5	27	IOCHRDY0 {IOCHRDY1}
8	Host data 10	28	Not connected
9	Host data 4	29	DACK0 {DACK1}
10	Host data 11	30	Ground
11	Host data 3	31	IRQ14
12	Host data 12	32	Not connected
13	Host data 2	33	Address 1
14	Host data 13	34	Not connected
15	Host data 1	35	Address 0
16	Host data 14	36	Address 2
17	Host data 0	37	Chip select 0
18	Host data 15	38	Chip select 1
19	Ground	39	Activity
20	Not connected	40	Ground

2-7-7 Disk On Module: IDE2(Slave)

Pin	Function	Pin	Function
1	Reset IDE	23	Slave IOW
2	Ground	24	Ground
3	Slave data 7	25	Slave IOR
4	Slave data 8	26	Ground
5	Slave data 6	27	Slave IOR
6	Slave data 9	28	Ground
7	Slave data 5	29	Slave ACK
8	Slave data 10	30	Ground
9	Slave data 4	31	IRQ15
10	Slave data 11	32	Not connected
11	Slave data 3	33	Slave data 1
12	Slave data 12	34	Not connected
13	Slave data 2	35	Address 0
14	Slave data 13	36	Address 2
15	Slave data 1	37	Chip select 0
16	Slave data 14	38	Chip select 1
17	Slave data 0	39	Activity
18	Slave data 15	40	Ground
19	Ground	41	+5V
20	Not connected	42	+5V
21	SDDREQ	43	Ground
22	Ground	44	Ground

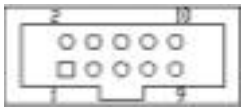
2-7-8 Parallel Port Connector: LPT1

This connector is used for parallel port.

Pin	Function	Pin	Function
1	Strobe	14	Auto Feed
2	Parallel data 0, PD0	15	Error
3	Parallel data 1, PD1	16	Initialize
4	Parallel data 2, PD2	17	Select
5	Parallel data 3, PD3	18	Ground
6	Parallel data 4, PD4	19	Ground
7	Parallel data 5, PD5	20	Ground
8	Parallel data 6, PD6	21	Ground
9	Parallel data 7, PD7	22	Ground
10	ACK, Acknowledge	23	Ground
11	Busy	24	Ground
12	Paper empty	25	Ground
13	Select	26	NC

2-7-9 Serial Port Connector: J4

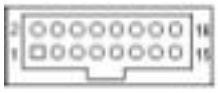
These 10-pin connectors are RS-232 ports used for serial communication.



Pin	Function	Pin	Function
1	DCD, Data carrier detect	2	DSR, Data set ready
3	RXD, Receive data	4	RTS, Request to send
5	TXD, Transmit data	6	CTS, Clear to send
7	DTR, Data terminal ready	8	RI, Ring indicator
9	GND, Ground	10	NC, Not connected

2-7-10 VGA CRT Connector : VGA1

This is a 15-pin connector used to connect the VGA CRT monitor.



Pin	Function	Pin	Function
1	Red	9	Vcc
2	Green	10	Ground
3	Blue	11	Not connected
4	Not connected	12	DDC data
5	Ground	13	HSYNC
6	Ground	14	VSYNC
7	Ground	15	DDC clock
8	Ground	16	NC

2-7-11 LAN Connector : J1,J2,J3(U8,U9,U10)

This connector allows you to connect to LAN, default setting is J1 to LAN3, J2 to LAN1 and J3 to LAN2.

Pin	Function	Pin	Function
1	TX+	5	N/C
2	TX-	6	RX-
3	RX+	7	N/C
4	N/C	8	N/C

2-7-12 Compact Flash : J5(IDE2-Master)

PIN No.	Signal Description	PIN No.	Signal Description
1	Ground	2	D3
3	D4	4	D5
5	D6	6	D7
7	CS#0	8	A10
9	ATA_SEL	10	A9
11	A8	12	A7
13	VCC	14	A6
15	A5	16	A4
17	A3	18	A2
19	A1	20	A0
21	D0	22	D1
23	D2	24	IOCS16
25	CD2	26	CD1
27	D11	28	D12
29	D13	30	D14
31	D15	32	CS1
33	VS1	34	IOR
35	IOW	36	WE#
37	INTRQ	38	VCC
39	CSEL	40	VS2
41	RESET	42	IOCHRDY
43	INPACK	44	REQ
45	DASP	46	PDIAG
47	D8	48	D9
49	D10	50	Ground

2-7-13 Power Connector –5V/-12V : J8.

PIN No.	Signal Description
1	-12V
2	GND
3	GND
4	-5V

2-7-14 Power Connector : J9.

PIN No.	Signal Description
1	+12V
2	GND
3	GND
4	+5V

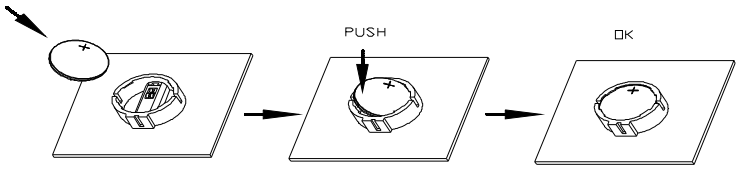
2-7-15 Battery Socket: BAT1

Follow below instructions and notice the caution for replacing and disposing of the RTC Lithium battery CR2032 for safety consideration :

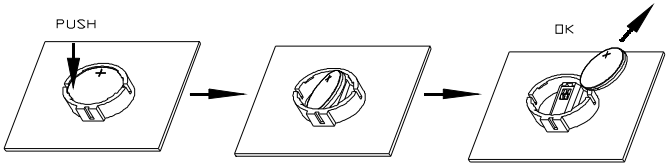
CAUTION:

- Danger of explosion if battery is incorrectly replaced.
- Replace only with the same or equivalent type recommended by the manufacturer.
- Dispose of used batteries according to the manufacturer's instruction.

(1) Install Battery Procedure

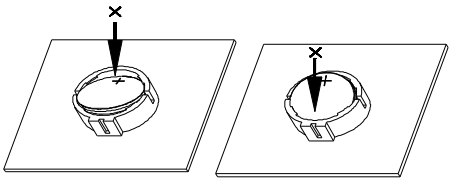


(2) Uninstall Battery Procedure



CAUTION:

- Do not install and press battery shown as below direction.



Chapter 3 System Installation

This chapter provides you with instructions on how to setup your system. The additional information shows you how to handle WDT operation in software program.

3.1 Memory

WEB-6681 Series provide onboard 64MB and 1 SO-DIMMs (144-pin Dual In-line Memory Module) to support 3.3V SDRAM (Synchronized DRAM) as on-board main memory. Onboard memory can be expansive up to 128MB by using 4 pieces of x16 type SDRAM. The maximum memory size of SO-DIMM is 32MB~ 512MB with using 16MB/32MB/64MB/128MB/256MB technology. Support up to 1 double-sided SO-DIMMs at 100/133MHz or 1 single-sided SO-DIMMs at 100/133MHz system memory bus. The memory architecture adopts 64-bit data interface to support for x16 SDRAM device width. In addition, it also supports Un-buffered , Non-ECC SDRAM and Enhanced Open page arbitration SDRAM paging scheme. For Refresh mechanism, the CBR ONLY supported.

For system compatibility and stability, don't use memory module without brand. You can also use the single or double-side SO-DIMM .The SO-DIMMs can be out of order. You can install different size of SDRAM module.

Without out the contact and lock integrity of memory module with socket, it will impact on the system reliability. Follow normal procedure to install your SDRAM module into memory socket. Before locking, make sure that the module has been fully inserted into the SO-DIMM slot.

NOTE: For maintaining system stability, do not change any of SDRAM parameters in BIOS setup to upgrade your system performance without acquiring technical information.

3.2 Installing the Embedded Board Computer

To install your WEB-6681 Series into the chassis or proprietary environment, you need to perform the following steps:

(1). Check all jumpers setting on proper position
(2). Install memory module on right position if necessary
(3). Place WEB-6681 Series into the dedicated position in your system
(4). Attach cables to existing peripheral devices and secure it

NOTE: Please refer section 3.3 to install display and Ethernet drivers and setup your system.

3.3 Install Display and Ethernet Driver

3-3-1 VIA VT8601A Integrated Graphics Controller

The on-board graphics controller is integrated in VIA VT8601A chipset that integrates 64-bit 2D/3D graphics accelerator in a single chip. The integrated graphics core with 2D, 3D and DVD video acceleration is fully matched with the mainstream requirement today. The optimized Shared Memory Architecture (SMA) can use system memory as frame buffer. The capacity is optional for 2~8MB and setup by BIOS setting. The graphics controller can support CRT resolution as 1280x1024x64K, 1024x768x16M, 800x600x16M and 640x480x16M colors.

3-3-2 Network Controller for Intel 82559 Intel 82559 ER or Realtek 8100BL Align

The Triple Intel 82559 or Intel 82559(ER) or REALTEK 8100BL is fully integrated 10BASE-T/100BASE-TX LAN solution. The 32-bit PCI controllers provide enhanced scatter-gather bus mastering capabilities and Enabled to perform high-speed data transfers over the PCI bus. Its bus master capabilities Enabled the component to process high level commands and perform multiple operations, which lower CPU utilization by off-loading communication tasks from the CPU.

The WEB-6681 Series provides two LED indicators on RJ-45 connectors to show LAN interface status. These messages will give you a guide for troubleshooting.

Yellow LED indicates transmit and receive activity.

Blinking : indicates transmit/receive activity

On : indicates no activity but link is valid

Off : link is invalid

Green LED indicates Link speed

On : link speed at 100Mbps

Off : link speed at 10Mbps

3-3-3 Drivers Support

WEB-6681 Series provides on CD-Title to support on-board VGA and Ethernet device drivers in various operating systems. Before installing the device drivers, please see the reference files in each sub-directory. **You cannot install drivers from CD-Title directly.**

- **VIA VT8601A CHIPSET INTEGRATED GRAPHICS: Support NT4.0, Windows9x/ME, Win2000, … environment**
- **VIA VT8601A and VT82C686B CHIPSET DRIVER: Support NT4.0, Windows9x, Win2000 , … environment**
- **REALTEK 8100BL: Support Dos, Windows3.1, Windows9x, NT3.5, NT4.0, Novell, OS/2 …**
- **Intel 82559: Support Dos, Windows3.1, Windows9x, NT3.5, NT4.0, Novell, OS/2 …**
- **Intel 82559(ER): Support Dos, Windows3.1, Windows9x, NT3.5, NT4.0, Novell, OS/2 …**

3-3-4 Watch-Dog Timer Programming

To activate the Watch-Dog Timer (WDT) function, you have to program I/O port 443H or 543H, reference to section 2.1. After this feature is enabled, a system reset will be generated unless an application triggers the timer periodically within time-out period. This allows the system to restart in an orderly way in case of any abnormal condition is found.

This WDT comes with 63 possible ranges of time intervals from 1s to 63sec., which can be adjusted by software programming. It could be enabled and programmed by writing I/O port 443H or 543H to issue trigger continuously, and disabled by programming the same port. A tolerance of 10% timer limit must be considered. For instance, if the time-out interval is set to 1 second, the WDT trigger command must be issued within 700ms at least.

The below example gives you a reference algorithm for WDT programming via I/O port 443H in your application programs:

Enable WDT

```
MOV     DX, 0443H ←— WDT port
MOV     AL, sec ←— sec = WDT time ( 1 < sec < 63sec.)
OUT     DX, AL
```

Re-trigger WDT

```
MOV     DX, 0443H ←— WDT port
MOV     AL, sec ←— sec = WDT time ( 1 < sec < 63sec.)
OUT     DX, AL
```

Disable WDT

```
MOV     DX, 0443H
MOV     AL, 0
OUT     DX, AL
```

Chapter 4 BIOS Setup Information

4.1 BIOS Setup Information

WEB-6681 Series is equipped with the AMI BIOS stored in Flash ROM. This BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it is retained during power-off periods. When system is turned on, WEB-6681 Series communicates with peripheral devices and check its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start-up.

4.2 Entering Setup

Turn on or reboot the computer. When the message “Hit <DEL> if you want to run SETUP” appears, press <Del> key immediately to enter BIOS setup program.

If the message disappears before you respond, but you still wish to enter Setup, please restart the system to try “COLD START” again by turning it OFF and then ON, or touch the "RESET" button. You may also restart from “WARM START” by pressing <Ctrl>, <Alt>, and <Delete> keys simultaneously. If you do not press the keys at the right time and the system will not boot, an error message will be displayed and you will again be asked to,

Press <F1> to Run SETUP or Resume

In HIFLEX BIOS setup, you can use the keyboard to choose among options or modify the system parameters to match the options with your system. The table below will show you all of keystroke functions in BIOS setup.

Key	Functions
Up Arrow	Move to the previous item
Down Arrow	Move to the next item
Left Arrow	Move to the item on the left (menu bar)
Right Arrow	Move to the item on the right (menu bar)
Move Enter	Move to the item you desired
Page Up key	Increase the numeric value or make changes
Page Down key	Decrease the numeric value or make changes
+ key	Increase the numeric value or make changes
- key	Decrease the numeric value or make changes
Esc key	Main Menu -- Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
F1 key	General help on Setup navigation keys
F10 key	Save all the CMOS changes and exit

4.3 Main Menu

Once you enter WEB-6681 Series AMI BIOS CMOS Setup Utility, you should start with the Main Menu ”Standard CMOS Setup”. The Main Menu allows you to select from eleven setup functions and two exit choices. Use arrow keys to switch among items and press

<Enter> key to accept or bring up the sub-menu.

AMIBIOS HIFLEX SETUP UTILITY - VERSION 1.54
(C)2001 American Megatrends, Inc. All Rights Reserved
Standard CMOS Setup
Advanced CMOS Setup
Advanced Chipset Setup
Power Management Setup
PCI / Plug and Play Setup
Peripheral Setup
Hardware Monitor Setup
Auto-Detect Hard Disks
Change User Password
Change Supervisor Password
Auto Configuration with Optimal Settings
Auto Configuration with Fail Safe Settings
Save Settings and Exit
Exit Without Saving
Standard CMOS setup for changing time, date, hard disk type, etc.
ESC:Exit ↑↓:Sel F2/F3:Color F10:Save & Exit

NOTE : It is strongly recommended to reload Optimal Setting if CMOS is lost or BIOS is updated**.**

4.4 Standard CMOS Setup Menu

This setup page includes all the items in a standard compatible BIOS. Use the arrow keys to highlight the item and then use the <Page Up>/<Page Down> or <+>/<-> keys to select the value or number you want in each item and press <Enter> key to certify it.

Follow command keys in CMOS Setup table to change Date, **Time, Drive type,** and **Boot Sector Virus Protection Status.**

- **Screen shot**

■ **Menu seletions**

Item	Options	Description
Date	MM : DD : YY	Set the system date. Note that the 'Day' automatically changes when you set the date
Time	HH : MM : SS	Set the system time
Drive A Drive B	Non Installed 360KB, 5 1/4 1.2MB, 5 1/4 720KB, 3 1/2 1.44MB, 3 1/2	Select the type of floppy disk drive installed in your system
Pri Master	Select a suitable item or keep it in Auto for automatic detection.	Press <Page Up> or <Page Down> to select a suitable item
Pri Slave	Select a suitable item or keep it in Auto for automatic detection.	Press <Page Up> or <Page Down> to select a suitable item
Sec Master	Select a suitable item or keep it in Auto for automatic detection.	Press <Page Up> or <Page Down> to select a suitable item
Sec	Select a suitable item or keep it in	Press <Page Up> or <Page Down> to select a

Slave	Auto for automatic detection.	suitable item

4.5 CMOS Setup Reference Table

This setup reference table includes all the Optimal, Failsafe, and Other options setting in each BIOS setup item. It is very easy to cross reference. If you want to go details, you can directly refer to item description in sub-section.

- **ADVANCED CMOS SETUP DEFAULTS**

BIOS Setup Items	Optimal Default	Failsafe Default	Other Options
Quick Boot	Enabled	Enabled	
1st Boot Device	IDE-0	IDE-0	IDE1, IDE2, IDE3.....
2nd Boot Device	IDE-1	IDE-1	IDE1, IDE2, IDE3.....
3rd Boot Device	CDROM	CDROM	IDE1, IDE2, IDE3.....
Try Other Boot Device	Yes	Yes	No
S.M.A.R.T. for Hard Disks	Disabled	Disabled	Enabled
Boot Up Num-Lock	On	On	Off
PS/2 Mouse Support	Enabled	Enabled	Disabled
Primary Display	VGA/EGA	VGA/EGA	Absent,…,Mono
Boot To OS/2	No	No	Yes
L1 Cache	Enabled	Enabled	Disabled
L2 Cache	Enabled	Disabled	Disabled
System BIOS Cacheable	Enabled	Disabled	Disabled
C000, 32K Shadow	Cached	Cached	Enabled, Disabled
C800, 16K Shadow	Disabled	Disabled	Cached, Enabled
CC00, 16K Shadow	Disabled	Disabled	Cached, Enabled
D000, 16K Shadow	Disabled	Disabled	Cached, Enabled
D400, 16K Shadow	Disabled	Disabled	Cached, Enabled
D800, 16K Shadow	Disabled	Disabled	Cached, Enabled
DC00, 16K Shadow	Disabled	Disabled	Cached, Enabled

- **ADVANCED CHIPSET SETUP DEFAULTS**

BIOS Setup Items	Optimal Default	Failsafe Default	Other Options
Configure SDRAM Timing by SPD	Disabled	Disabled	Enabled
DRAM Frequency	100Mhz	100Mhz	133Mhz ,66Mhz
SDRAM CAS# Latency	3	3	2
DRAM Bank Interleave	Enabled	Disabled	Enabled
DRAM Integrity Mode	Disabled	Disabled	Enabled
Memory Hole	Disabled	Disabled	512KB-640KB, 15MB-16MB, 14MB-16MB
AGP Mode	4x	2x	1x
AGP fast Write	Disabled	Disabled	Enabled

AGP Aperture Size	64MB	64MB	4,8,16,32,128,256MB
Search for MDA Resources	Yes	No	
PCI Delay Transaction	Enabled	Disabled	
ISA Bus Clock	PCICLK4	PCICLK/4	PCICLK/2,PCICLK3, PCICLK/5,PCICLK6
USB Controller	All USB Port	Disabled	USB Port 0&1, USB Port 2&3.
USB Device Legacy Support	All Device	All Device	No mice, Disabled
Spread Spectrum Controller	Normal	Normal	Enabled
Spread Spectrum Modulation	0.25%	0.25%	0.5%

● POWER MANAGEMENT SETUP DEFAULTS

BIOS Setup Items	Optimal Default	Failsafe Default	Other Options
ACPI Aware O/S	Yes	Yes	No
Power Management / APM	Enabled	Disabled	Disabled
Video Power Down Mode	Suspend	Disabled	Stand By
Hard Disk Power Down Mode	Stand By	Disabled	Suspend
Standby Time Out (Minute)	Disabled	Disabled	1, 2, 4, 8, 10, 20, 30, 40, 50, 60 .
Suspend Time Out (Minute)	Disabled	Disabled	1, 2, 4, 8, 10, 20, 30, 40, 50, 60 .
Throttle Slow Clock Ratio	50 %-56.25%	50 %-56.25%	0%-6.25%, 6.25%-12.5%, 18.75%-25%, 31.25%- 37.5%, 37.5%-43.75% 43.75%-50% 56.25%-62.5% 62.5%-68.75% 68.75%-75% 75%-87.5% 75%-81.25% 81.25%-87.5% 87.5%-93.75% 93.75%-100%
Display Activity	Ignore	Ignore	Monitor
IRQ3	Monitor	Ignore	Ignore
IRQ4	Monitor	Ignore	Ignore
IRQ5	Ignore	Ignore	Monitor
IRQ7	Monitor	Ignore	Ignore
IRQ9	Ignore	Ignore	Monitor
IRQ10	Ignore	Ignore	Monitor
IRQ11	Ignore	Ignore	Monitor
IRQ13	Ignore	Ignore	Monitor
IRQ14	Monitor	Ignore	Ignore
IRQ15	Ignore	Ignore	Monitor

● PCI / Plug AND Play SETUP

BIOS Setup Items	Optimal Default	Failsafe Default	Other Options
Plug and Play Aware O/S	No	No	Yes
Clear NVRAM	No	No	Yes
On board 1 st LAN	Enabled	Enabled	Disable
On board 2 st LAN	Enabled	Enabled	Disable
On board 3 st LAN	Enabled	Enabled	Disable
On Chip VGA Fram Buffer Size	8MB	8MB	None,2,4,16.32MB
PCI Latency Timer (PCI Clocks)	32	32	64, 96, 128, 160, 192, 224, 248
Primary Graphics Adapter	On Chip VGA	On Chip VGA	PCI
Boot Screen Select	Auto	Auto	Both CRT & LCD,
LCD Panel Type	0	0	1 ~ 15
Allocate IRQ to PCI VGA	Yes	Yes	No
PCI IDE Bus Master	Disabled	Disabled	Enabled
DMA Channel 0	PnP	PnP	ISA/ EISA
DMA Channel 1	PnP	PnP	ISA/ EISA
DMA Channel 3	PnP	PnP	ISA/ EISA
DMA Channel 5	PnP	PnP	ISA/ EISA
DMA Channel 6	PnP	PnP	ISA/ EISA
DMA Channel 7	PnP	PnP	ISA/ EISA
IRQ3	PCI/ PnP	PCI/ PnP	ISA/ EISA
IRQ4	PCI/ PnP	PCI/ PnP	ISA/ EISA
IRQ5	PCI/ PnP	PCI/ PnP	ISA/ EISA
IRQ7	PCI/ PnP	PCI/ PnP	ISA/ EISA
IRQ9	PCI/ PnP	PCI/ PnP	ISA/ EISA
IRQ10	PCI/ PnP	PCI/ PnP	ISA/ EISA
IRQ11	PCI/ PnP	PCI/ PnP	ISA/ EISA
IRQ12	PCI/ PnP	PCI/ PnP	ISA/ EISA
IRQ14	PCI/ PnP	PCI/ PnP	ISA/ EISA
IRQ15	PCI/ PnP	PCI/ PnP	ISA/ EISA

● PERIPHERAL SETUP DEFAULTS

BIOS Setup Items	Optimal Default	Failsafe Default	Other Options
On Board Serial Port1	Auto	Auto	Disabled 3F8h/COM1, 2F8h/COM2, 3E8h/COM3, 2E8h/COM4,
On Board Parallel Port	Auto	Auto	Disabled, 378, 278, 3BC
Parallel Port Mode	Normal	Normal	Normal, EPP, Bi-Dir ECP, EPP+ECP
EPP Version	N/A	N/A	
Parallel Port DMA Channel	N/A	N/A	
Parallel Port IRQ	Auto	Auto	

On Board IDE	Both	Both	Disabled, Primary , Secondary ,Reserved

- **HARDWARE MONITOR SETUP DEFAULT**

BIOS Setup Items	Optimal Default	Failsafe Default	Other Options
..CPU Temperature	===		
System Temperature	===		
CPU Fan Speed	===		
Vcore	===		
+ 2.500V	===		
+ 3.300V	===		
+ 5.000V	===		
+ 12.000V	===		

4.6 Standard CMOS Setup Menu

This setup page includes all the items in a standard compatible BIOS. Use the arrow keys to highlight the item and then use the <Page Up>/<Page Down> or <+>/<-> keys to select the value or number you want in each item and press <Enter> key to certify it.

Follow command keys in CMOS Setup table to change **Date, Time, Drive type**, and **Boot Sector Virus Protection Status**.

4.7 Advanced CMOS Setup Menu

This setup includes all of the advanced features in the system. The detail descriptions are specified as below.

Quick Boot

Set “Disabled” for normal booting or select “Enabled” to skip minor BIOS test items to obtain quick boot response.

Boot Up Sequence

This category includes six items to determine which drive computer searches first for the Disk Operating System (DOS).

The default ARMD (ATAPI Removable Media Device) emulation type is set to popular drive type LS-120 and ATAPI ZIP. There are many choices of booting devices to boot up system. User can select “Disabled”, “IDE-0”, “IDE-1”, “IDE-2”, “IDE-3”, “Floppy”, “ARMD-FDD”, “ARMD-HDD”, “CDROM”, “SCSI”, or “NETWORK”.

Try Other Boot Device

Select “Yes” to Enabled trying to boot from different devices in sequence. Selected “No” for booting only from the first boot device.

S.M.A.R.T for Hard Disks

Self-Monitoring, analysis and reporting Technology. For prediction of device degradation and/or faults.

Boot Up Num-Lock

Select “On” to Enabled numeric function of the numeric keypad, or “Off” to disregard it.

PS/2 Mouse Support

Select “Enabled” to Enabled PS/2 mouse function, or “Disabled” to release IRQ12 interrupt for other ISA-bus I/O devices.

System Keyboard

This option will be used to neglect “keyboard error” while you choose Absent setting in your BIOS setup and system has no keyboard attached.

Primary Display

Chooses Absent, VGA/EGA, CGA40x25, CGA80x25, or Mono to meet your monitor type. If you select Absent, the “CMOS Display Type Wrong” message will be ignored regardless the mismatched display card.

Password Check

This option Enables the password checking when the system boots up or runs CMOS Setup. It only takes effect after setting Change Supervisor Password.

Setup : This option will force system to check password before running Setup if you have already entered the current user password in "Change User Password". By that time, the system will be only able to boot but deny accessing Setup.

Always : Password prompt appears every boot-up. The system will not boot and deny access Setup with invalid password. The best way is to clear CMOS or try to reload BIOS Setup to boot up system.

Boot To OS/2

You should set this option to "Yes" to support OS/2 environment.

L1 Cache

This option controls to turn on or off the CPU's Level 1 built-in cache.

L2 Cache

Enabled his option to turn on or off the CPU's Level 2 built-in cache.

System BIOS Cacheable

Enabled this option to enhance system performance by shadowing and caching system BIOS. When disabled, this BIOS shadow function will be ignored.

Shadow Memory

Each of segments provides three options "Disabled", "Enabled", and "Cached" for faster adapter's ROM execution. However this shadow function is Chipset oriented and dependent on system hardware feature. In general, C000 64k will be allocated for VGA BIOS and set to Cached to get higher display performance by shadowing and caching feature. If user chooses Enabled setting, only BIOS shadow function is active.

4.8 Advanced Chipset Setup Menu

NOTE ：This setup is very important to keep system stability. If you are not technical person, do not attempt to change any parameters. The best way is to choose optimal default setting.

Configure SDRAM Timing by SPD

This option provides DIMM plug-and-play support by Serial Presence Detect (SPD) mechanism via the System Management Bus (SMBus) interface. You can disable this option to manage the following four SDRAM timing options by yourself. In addition, SDRAM operating timings may follow serial presence from EEPROM content by setting this option to “Enabled”, and all of SDRAM timing options will be not available and hidden.

DRAM Frequency

PC-100 means the memory bus is running at 100MHz. PC-133 means its bus is running at 133MHz.

SDRAM CAS# Latency

This option controls the number of SCLKs between the time a read command is sampled by the SDRAMs and the time the North Bridge, 8601A, samples correspondent data from the SDRAMs.

Spread Spectrum

This option is for EMI test only.

Memory Hole

This option allows the end users to specify the location of a memory hole for memory space requirement from ISA-bus cards.

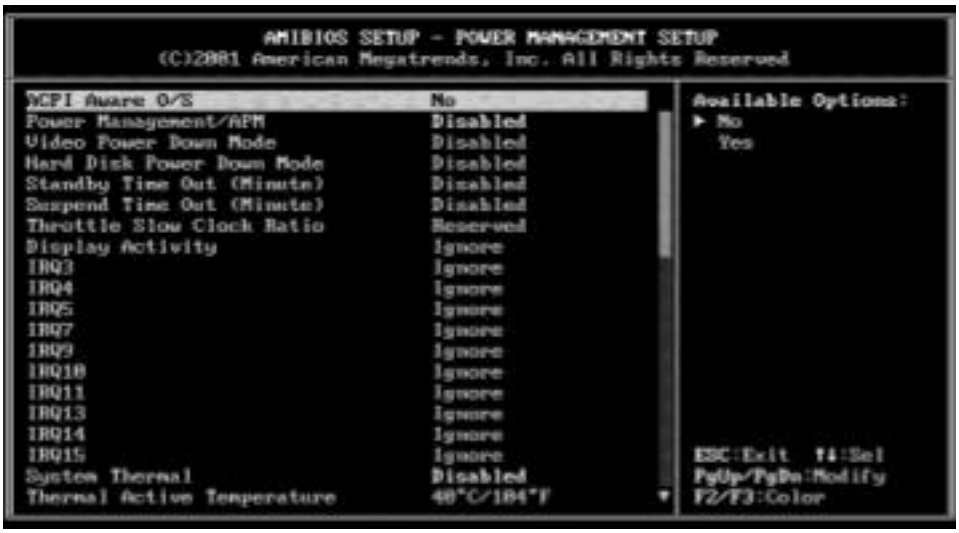
USB Controller

This option will Enabled on-chip USB function to support USB peripheral devices.

USB Device Legacy Support

This feature will be automatically disabled and hidden if user chooses the "Disabled" setting from the foregoing USB Function option. Otherwise, enabling this option provides support for USB-keyboard without auxiliary driver under DOS environment.

4.9 Power Management Setup Menu



This APM (Advanced Power Management) determines how much power energy can be saved by setting below items to handle system power resource. The following descriptions will specify the definition of each item in details.

Power Management/APM

Using this feature to control system power resources. Set this option to "Enabled" to Enabled power management function and effective based on following parameter settings.

Video Power Down Mode

This option specifies the power conserving state that the VESA VGA video subsystem enters after the specified period of display inactivity has expired.

Hard Disk Power Down Mode

This option specifies the power management state that the HDD enters after the specified period of hard drive inactivity has expired. It is the same as video power control. If user chooses “Stand By” or “Suspend”, it will depend on period of parameter “Stand By Time out” or “Suspend Time out”.

Stand by Time out (Minute)

This option specifies the length of the period of system inactivity while the computer is in Full-On power state before the computer is placed in Standby mode. When this length of time expires, the computer enters Standby Timeout state. In Standby mode, some power use is curtailed.

Suspend Time out (Minute)

This option is the same as Stand by Time out function. These two features will be Enabled to monitor power of sub-items “Display Activity”, “Serial port”, “Parallel Port”, “Floppy”, “Pri-HDD”, and “Sec-HDD” independently. It is also used to control CPU throttle running function. All of sub-items will be ineffective in selection of disabling “Stand by Time out” or “Suspend Time out” even if it can be choose by user in BIOS setup menu.

Throttle Slow Clock Ratio

This option specifies the speed at which the system clock runs in power saving modes. The settings are expressed as duty cycle of the STPCLK# signal. This duty cycle indicates the percentage of time the STPCLK# signal is asserted while in the throttle mode.

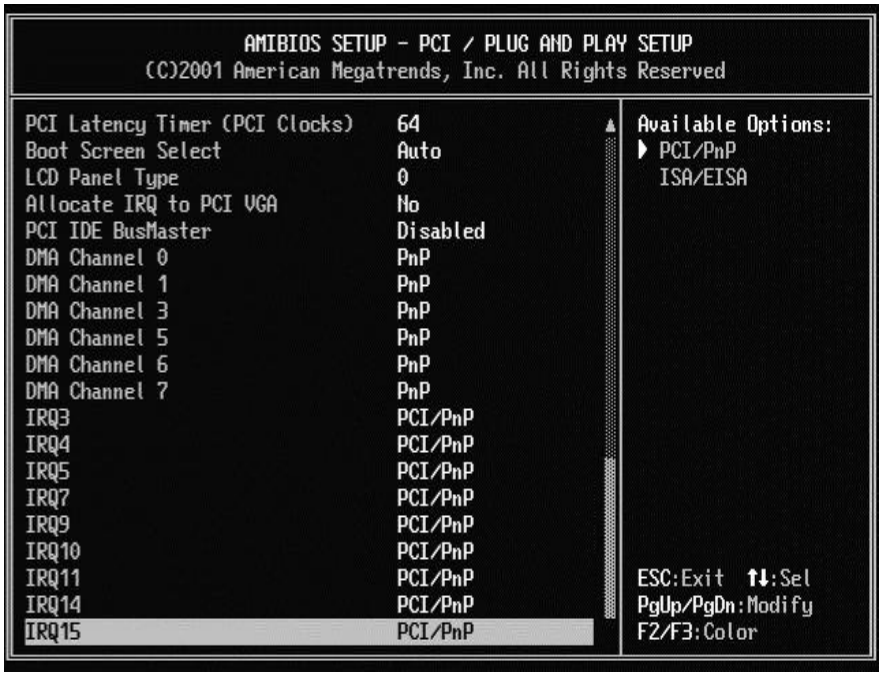
Display Activity

This option specifies if BIOS is to monitor activity on the display monitor for power conservation purposes. If set to Monitor and the computer is in a power saving state, BIOS watches for video display activity. The computer enters the full on power state if any activity occurs. BIOS reloads the Standby and Suspend timeout timers if activity occurs on the specified IRQ lines. If set to Ignore, video display monitor activity is not monitored.

IRQ Active

When set to Monitor, these options Enabled event monitoring on the specified IRQ. If set to Monitor and the computer is in a power saving state, BIOS watches for activity on the device with specified IRQ line. The computer enters the full on power state if any activity occurs. BIOS reloads the Standby and Suspend timeout timers if activity occurs on the specified IRQ. No monitoring activity occurs if the option is set to Ignore. The settings for each of these options are Monitor or Ignore.

4.10 PCI/Plug and Play Setup



This section describes configuring the PCI bus system. PCI (Peripheral Component Interconnect) is a system which allows I/O devices to operate at speeds nearing CPU's when they communicate with own special components.

All of options described in this section are important and technical and it is strongly recommended that only experienced users could make any changes to the default settings.

Plug and Play Aware O/S

Set this option to “Yes” if the operating system installed in the computer is Plug and Play-aware. BIOS only detects and Enabled PnP ISA adapter cards that are required for system boot. The Windows 95 operating system detects and Enabled all other PnP-aware adapter cards. Windows 95 is PnP-aware. Set this option to “No” if the operating system (such as DOS, OS/2, Windows 3.x) does not use PnP. You must set this option correctly or PnP-aware adapter cards installed in your computer will not be configured properly.

Clear NVRAM

This option is used to clear NVRAM and check or update ESCD (Extended System Configuration Data) data after system power on. Set this option to No that will not clear NVRAM and the operation of update ESCD is effective in different ESCD data comparison. If you select the “Yes” setting, then the BIOS will update ESCD each time of power on.

On Board(1st,2nd,3rd)LAN

These options are Enabled or disable LAN function.

PCI Latency Timer (PCI Clocks)

This option is used to control PCI latency timer period (follow PCI clocks). Based on PCI specification 2.1 or later and PCI bus frequency in system, user can select different timer to meet their PCI bus environment.

PCI VGA Palette Snoop

Some display cards that are non-standard VGA such as graphics accelerations or MPEG video cards may not show colors properly. User can choose "Enabled" setting to correct this display mismatch problem and support any ISA adapter card installed in the computer requires VGA palette snooping.

Allocate IRQ to PCI VGA

This option will be used to allocate IRQ for PCI VGA card. In general, some of PCI VGA cards need IRQ support.

PCI IDE Bus Master

Set this option to Enabled to specify that the IDE controller on the PCI local bus has bus mastering capability.

DMA Channel 0/1/3/5/6/7

These options specify if the named DMA channel is available for using on the ISA/EISA bus or PnP (Plug & Play).

IRQ 3/4/5/7/9/10/11/12/14/15

These options specify the bus that the named interrupt request lines (IRQs) are

used on. These options allow you to specify IRQs for use by legacy ISA adapter cards. These options determine if AMIBIOS should remove an IRQ from the pool of available IRQs passed to devices that are configurable by the system BIOS. The available IRQ pool is determined by reading the ESCD NVRAM. If more IRQs must be removed from the pool, the end user can use these PCI/PnP Setup to remove the IRQ by assigning the option to the ISA/EISA setting. All IRQs used by on-board I/O are configured as PCI/PnP.

4.11 Peripheral Setup

This section describes I/O resources assignment for all of on-board peripheral devices.

On Board Serial Port 1

These fields control the resource assignments of two on-board serial interfaces SIO1 and SIO2. The following lists show current options in On Board Serial Port 1/ Port 2 :

Auto → cannot set serial I/O resources by manual operation
Disabled → indicates on-board COM port function is ineffective
3F8h/COM1 → assign I/O address 3F8h to COM1
2F8h/COM2 → assign I/O address 2F8h to COM2
3E8h/COM3 → assign I/O address 3E8h to COM3
2E8h/COM4 → assign I/O address 2E8h to COM4

On Board Parallel Port

There are four optional items Parallel Port Mode, EPP Version, Parallel Port IRQ, and Parallel Port DMA Channel used to control on-board parallel port interface while user select I/O base address manually. The following lists are available options of on-board parallel port :

Auto → user can not control all of LPT port I/O resources

Disabled → on-board parallel port function is ineffective and N/A

378h → locate IRQ7 for this default I/O address

278h → assign this I/O address to LPT1

3BCh → assign this I/O address to LPT1

◎ **Parallel Port Mode :**

This option specifies the parallel port mode. ECP and EPP are both bi-directional data transfer schemes that adhere to the IEEE P1284 specifications. This Parallel Port Mode includes four options “Normal”, “Bi-Dir”, “EPP”, and “ECP”.

Setting	Description
Normal	Uni-direction operation at normal speed
Bi-Dir	Bi-direction operation at normal speed
EPP	The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bi-directional data transfer driven by the host device.
ECP	The parallel port can be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve data transfer rates up to 2.5 Megabits per second. ECP provides symmetric bi-directional communication.

- **EPP Version :**

This option is only valid if the Parallel Port Mode option is set to EPP. This

option specifies the version of the Enhanced Parallel Port specification that will be used by AMIBIOS.

- **Parallel Port DMA Channel :**

  This option is only available if **On Board Parallel Port** is set to fixed I/O address and the setting of Parallel Port Mode is ECP. This option sets the DMA channel used by ECP-capable parallel port.

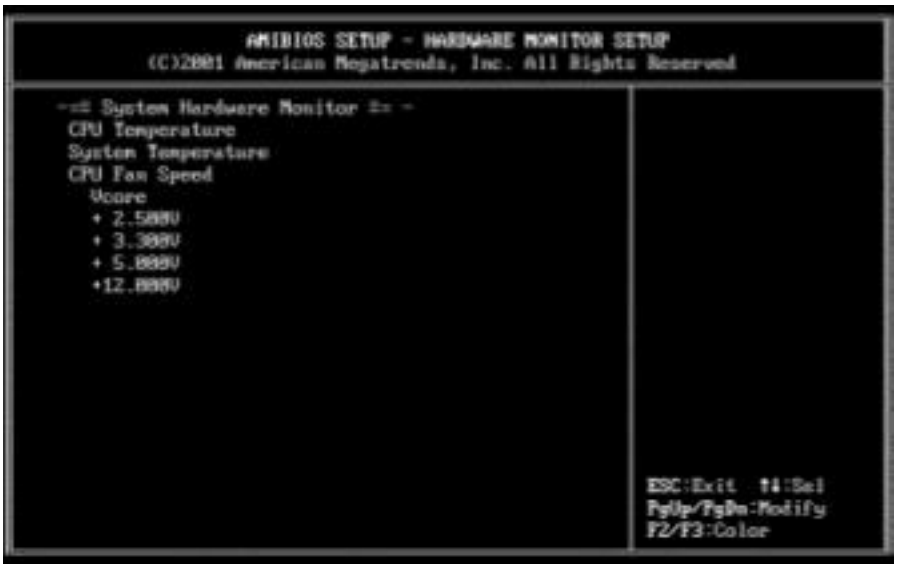
- **Parallel Port IRQ :**

  This option is only valid if the **Onboard Parallel Port** option is not set to *Disabled*. This option sets the IRQ used by the parallel port.

On Board IDE

This option specifies the onboard IDE controller channels that will be used. The settings are Disabled, Primary, Secondary, or Both.

4.12 Hardware Monitor Setup



This setup describes current system status detected from hardware monitor controller. The status showed on screen will include :

- There are two on-board temperature sensors, TSENS1, and TSENS2.
- Current System Temperature (Generally indicates the inside temperature of chassis or surface temperature of SBC)
- Current CPU Fan Speed
- Current Chassis Fan Speed
- System operating voltage includes “CPU Vcore”, “+2.500V”, “+3.300”, “+5.000V”, “+12.000V”.

4.13 BIOS POST Check Point List

AMIBIOS provides all IBM standard Power On Self Test (POST) routines as well as enhanced AMIBIOS POST routines. The POST routines support CPU internal diagnostics. The POST checkpoint codes are accessible via the Manufacturing Test Port (I/O port 80h).

Whenever a recoverable error occurs during the POST, the system BIOS will display an error message describing the message and explaining the problem in detail so that the problem can be corrected.

During the POST, the BIOS signals a checkpoint by issuing one code to I/O address 80H. This code can be used to establish how far the BIOS has executed through the power-on sequence and what test is currently being performed. This is done to help troubleshoot faulty system board.

If the BIOS detects a terminal error condition, it will halt the POST process and attempt to display the checkpoint code written to port 80H. If the system hangs before the BIOS detects the terminal error, the value at port 80H will be the last

test performed. In this case, the terminal error cannot be displayed on the screen. The following POST checkpoint codes are valid for all AMIBIOS products with a core BIOS date of 07/15/95 version 6.27 (Enhanced).

Uncompressed Initialization Codes — The uncompressed initialization checkpoint hex codes are listed in order of execution :

Code	Description
D0	NMI is disabled. CPU ID saved. INIT code checksum verification will be started.
D1	Initializing the DMA controller, performing the keyboard controller BAT test, starting memory refresh, and going to 4GB flat mode.
D3	To start memory sizing.
D4	Returning to real mode. Executing any OEM patches and setting the stack next.
D5	Passing control to the uncompressed code in shadow RAM at E000:0000h. The INIT code is copied to segment 0 and control will be transferred to segment 0.
D6	Control is in segment 0. Next, checking if <Ctrl><Home> was pressed and verifying the system BIOS checksum. If either <Ctrl><Home> was pressed or the system BIOS checksum is bad, next will go to checkpoint code E0h. Otherwise, going to checkpoint code D7h.
D7	To pass control to interface module.
D8	Main BIOS runtime code is to be decompressed.
D9	Passing control to the main system BIOS in shadow RAM next.

Boot block Recovery Codes — The boot block recovery checkpoint hex codes are listed in order of execution :

Code	Description
E0	The onboard floppy controller if available is initialized. Next, beginning the base 512KB memory test.
E1	Initializing the interrupt vector table next.

Code	Description
E2	Initializing the DMA and Interrupt controllers next.
E6	Enabling the floppy drive controller and Timer IRQs. Enabling internal cache memory.
ED	Initializing the floppy drive.
EE	Start looking for a diskette in drive A: and read first sector of the diskette.
EF	A read error occurred while reading the floppy drive in drive A: .
F0	Next, searching for the AMIBOOT.ROM file in the root directory.
F1	The AMIBOOT.ROM file is not in the root directory.
F2	Next, reading and analyzing the floppy diskette FAT to find the clusters occupied by the AMIBOOT.ROM file.
F3	Start reading AMIBOOT.ROM file, cluster by cluster.

F4	The AMIBOOT.ROM file is not the correct size.
F5	Next, disabling internal cache memory.
FB	Next, detecting the type of Flash ROM.
FC	Erasing the Flash ROM.
FD	Programming the Flash ROM
FF	Flash ROM programming was successful. Next, restarting the system BIOS.

Uncompressed Initialization Codes — The following runtime checkpoint hex codes are listed in order of execution. These codes are uncompressed in F0000h shadow RAM.

Code	Description
03	The NMI is disabled. Next, checking for a soft reset or a power on condition.
05	The BIOS stack has been built. Next, disabling cache memory.
06	Uncompressing the POST code next.
07	Next, initializing the CPU and the CPU data area.
08	The CMOS checksum calculation is done next.
0B	Next, performing any required initialization before the keyboard BAT command is issued.
0C	The keyboard controller input buffer is free. Next, issuing the BAT command to the keyboard controller.
0E	The keyboard controller BAT command result has been verified. Next, performing any necessary INIT after the K/B controller BAT command test.
0F	The keyboard command byte is written next.
10	Next, issuing the pin 23 and 24 blocking and unblocking commands.
11	Next, checking if the <End> or <Ins> keys were pressed during power on.
12	To initialize CMOS if the *initialize CMOS RAM in every boot* is set or the <End> key is pressed. Going to disable DMA and Interrupt controllers.
13	The video display has been disabled. Port B has been initialized. Next, initializing the chipset.

Code	Description
14	The 8254 timer test will begin next.
19	The 8254 timer test is over. Starting the memory refresh test next.
1A	The memory refresh line is toggling. Checking the 15us on/off time next.
23	Reading the 8042 input port and disabling the MEGAKEY Green PC feature next. Making the BIOS code segment writable and performing any necessary configuration before initializing the interrupt vectors.
24	The configuration or setup required before interrupt vector initialization has completed. Interrupt vector init. is about to begin
25	Interrupt vector initialization is done. Clearing the password if the POST

	DIAG switch is on.
27	Any initialization before setting video mode to be done.
28	Going for monochrome mode and color mode setting.
2A	Bus initialization system, static, output devices will be done next, if present.
2B	Passing control to the video ROM to perform any required configuration before the video ROM test.
2C	To look for optional video ROM and give control.
2D	The video ROM has returned control to BIOS POST. Performing any required processing after the video ROM had control.
2E	Completed post-video ROM test processing. If the EGA/VGA controller is not found, performing the display memory read/write test next.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. Look for retrace checking next.
31	Display memory R/W test or retrace checking failed. To do alternate display retrace checking.
32	Alternate display memory R/W test passed. To look for the alternate display retrace checking.
34	Video display checking is over. Setting the display mode next.
37	The display mode is set. Displaying the power on message next.
38	Initializing the bus input, IPL, and general devices next, if present.
39	Displaying bus initialization error message.
3A	The new cursor position has been read and saved. Displaying the *Hit <DEL>* message next.
40	Preparing the descriptor tables next.
42	Entering protected mode for the memory test next.
43	Entered protected mode. Enabling interrupts for diagnostics mode next.
44	Interrupts Enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next.
45	Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next.
46	The memory wraparound test has completed. The memory size calculation has been done. Writing patterns to test memory next.
47	The memory pattern has been written to extended memory. Writing patterns to the base 640 KB memory test.

Code	Description
48	Patterns written in base memory. Determining the amount of memory below 1MB next.
49	The amount of memory below 1MB has been found and verified. Determining the amount of memory above 1MB memory next.
4B	The amount of memory above 1MB has been found and verified. Checking for a soft reset and clearing the memory below 1MB for the soft reset next. If this is a power on situation, going to checkpoint 4Eh next.
4C	The memory below 1MB has been cleared via a soft reset. Clearing the memory above 1MB next.
4D	The memory above 1MB has been cleared via soft reset. Saving the memory

	size next. Going to checkpoint 52h next.
4E	The memory test started, but not as the result of a soft reset. Displaying the first 64KB memory size next.
4F	Memory size display started. This will be updated during memory test. Performing the sequential and random memory test next.
50	Memory testing/initialization below 1MB completed. Going to adjust displayed memory size for relocation and shadowing.
51	The memory size display was adjusted for relocation and shadowing. Testing the memory above 1MB next.
52	The memory above 1MB has been tested and initialized. Saving the memory size information next.
53	The memory size information and the CPU registers are saved. Entering real mode next.
54	Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next.
57	The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next.
58	The memory size was adjusted for relocation and shadowing. Clearing the *Hit <DEL>* message next.
59	The *Hit <DEL>* message is cleared. The *<WAIT…>* message is displayed. Staring the DMA and interrupt controller test next.
60	The DMA page register test passed. To do DMA#1 base register test.
62	DMA#1 base register test passed. To do DMA#2 base register test.
65	DMA#2 base register test passed. To program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller.
7F	Extended NMI sources enabling is in progress.
80	The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next.
81	A keyboard reset error or stuck key was found. Issuing the keyboard Controller interface test command next.
82	The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
83	Command byte written, Global data init done. To check for lock-key.
84	Locked key checking is over. Checking for a memory size mismatch with CMOS RAM data next.
85	The memory size check is done. Displaying a soft error and checking for a password or bypassing Setup next.
86	Password checked. About to do programming before setup.
87	The programming before Setup has completed. Uncompressing the Setup code and executing the AMIBIOS Setup utility next.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	The programming after Setup has completed. Displaying the power on Screen message next.
8B	The first screen message has been displayed. The <WAIT…> message is displayed. Performing the PS/2 mouse check and extended BIOS data

	area allocation check next.
8C	Programming the Setup options next.
8D	Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	The floppy drive controller has been configured. Configuring the hard disk drive controller next.
95	Initializing the bus option ROMs from C800 next.
96	Initializing before passing control to the adaptor ROM at C800.
97	Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next.
98	The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.
99	Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next.
9C	Required initialization before the Coprocessor test is over. Initializing the Coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after Coprocessor test.
9E	Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next.
A2	Displaying any soft errors next.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Memory wait state programming is over. Clearing the screen and enabling parity and the NMI next.
A7	NMI and parity Enabled. Performing any initialization required before passing control to the adaptor ROM at E000 next.
A8	Initialization before passing control to the adaptor ROM at E000h completed. Passing control to the adaptor ROM at E000h next.
A9	Returned from adaptor ROM at E000h control. Performing any initialization required after the E000 option ROM had control next.
AA	Initialization after E000 option ROM control has completed. Displaying the system configuration next.
AB	Building the multiprocessor table, if necessary.
AC	Uncompressing the DMI data and initializing DMI POST next.
B0	The system configuration is displayed.
B1	Copying any code to specific areas.
00	Code copying to specific areas is done. Passing control to INT 19 h boot loader next.

4.14 Flash BIOS Utility

Utilize AMI Flash BIOS programming utility to update on-board BIOS for the future new BIOS version. Please contact your technical window to get this utility if necessary.

NOTE : Remark or delete any installed Memory Management Utility (such as HIMEM.SYS, EMM386.EXE, QEMM.EXE, …, etc.) in the CONFIG.SYS files before running Flash programming utility.